Intel Labs

Microarchitecture and Circuits

Developing New Designs for Greater Performance and Power

What other ways besides speed can we increase the performance of a microprocessor? How do we factor in the effects of quantum physics in designing a chip to be manufactured on the nanometer scale? How can we optimize microarchitecture to improve chip performance as developers shift to dynamic programming languages like C# and Java? New challenges call for new thinking. At Intel Labs we're finding innovative ways to enhance processor performance and enable new uses of computing through microarchitecture and circuit design. We're also doing ground-breaking work characterizing tomorrow's applications to ensure our processor designs truly forge the future.

Building a New Paradigm for Performance

Having already adapted to the microscale many of the best mainframe features and designs, we're now pioneering novel microarchitectures and technologies in the Intel® Pentium® 4 processor line and beyond. Probably the biggest design challenges we face in coming years involve the shift in scale from micrometers to nanometers, working in dimensions as small as three atoms wide. At the same time, power consumption has become an issue and we're looking for ways to get the maximum performance out of a processor within an appropriate power window for the form factor. Low-power architectures like the Mobile Intel Pentium III-M processor are a perfect example. To achieve these new levels of power efficiency and performance, we're doing major research in multithread microarchitecture, finding ways of executing multiple independent instruction strings at the same time within one processor or multiple processors. We're also investigating ways to speed up processor performance by improving the selection of data that gets stored in memory and which memory it gets stored in. To help processors improve their ability to predict what data software will need next, we're exploring novel instruction supply and prediction techniques, and techniques for bypassing memory latency and improving memory hierarchy organization.

The Circuits of Tomorrow

As processor performance moves in the multi-gigahertz range, matching performance gains need to be made in interchip and interboard communication speeds to prevent bottlenecks there. We're looking into faster ways of moving data within a chip, between chips, between chips and devices, and between systems and subsystems in different chassis. Probably the area with the greatest potential for a quantum performance leap is optical signaling at the micro level. We're researching building lasers into silicon to move data between chips and devices at fiber optic speeds, moving photons instead of electrons. We're also making significant advances in power-optimized circuit technology and high performance and power-efficient data path circuits — an area where we're combating power leakage with several novel logic elements that can be used to equal or exceed the performance of conventional circuits while using half the number of devices and

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half the susceptivity to power leakage. In high-speed signaling for microprocessor communication, we're researching ways to enhance simultaneous bi-directional signaling technology, particularly low-cost solutions to reaching multi-gigahertz clocking rates over wide busses and longer distances. In servers, high-speed signaling is rapidly growing in importance as a way to increase network performance through faster communication within a rack.

Programming New Ways to High Performance

In the labs, a major part of our work is characterizing future applications and programming system workloads so our microarchitecture and circuit designs will meet the needs of tomorrow's applications. Anticipating the need for new ways to speed up programs like databases and multimedia applications, we're exploring speculative multithreading. This technique anticipates the need for seldom used pieces of data and pre-loading them in memory. We're also preparing for a future where dynamic compiling programs, specifically Java and C#, are the dominant application programming languages. We're performing systems research in dynamic compilation and memory management for these programs. For software developers, we're working on techniques for applications to improve their performance dynamically for our processors. The Dynamic Optimization Project is building a way to use the hardware performance monitor within the Intel® Itanium™ processor to closely monitor an application's run-time execution behavior and identify problematic regions as candidates for run-time optimizations in a software-based dynamic optimizer. These optimizations are performed on the fly to improve the overall performance of the application.

The Shape of Things to Come

The work we're doing in microarchitecture and circuits now should have a major impact on the next decade. We should see new ways of defining performance in microprocessors beyond gigahertz. We should see more power-efficient microprocessors in everything from the mobile computer on your lap to the buildings all over the world containing the racks of servers holding and exchanging the data of the Internet economy. We should see new advances in circuitry that move data at ever-increasing speeds within and outside the microprocessors. We should see new advances in compiler technologies, memory optimization and dynamic optimization techniques that speed the development of applications for each generation of microprocessor and even tune application performance for how individual people use an application.

About Intel Labs

Intel Labs are the R&D arm of Intel. We have more than 6,000 researchers and scientists in 80 labs around the world. Our decentralized structure allows us to tackle a broad range of research projects. The labs are closely aligned with Intel's business units and focus on R&D for technologies and products that specifically address the needs of our customers.

Designing the Future

Find out more about Intel Labs by visiting www.intel.com/labs. The digital world of tomorrow is in our labs today.

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